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HAMILTON & TERRILE, LLP
P.O. BOX 203518
AUSTIN, TX 78720

EXAMINER	
MEREDITH, LEONARD E	
ART UNIT	PAPER NUMBER
2109	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,254	LARSON ET AL.	
	Examiner	Art Unit	
	Leonard Meredith	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).*

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 05/25/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Stern et al. (Pat. Pub. US 2004/0181656).

With respect to Claim 1, Stern et al. recites a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Initiating startup, determining memory test required, generating test data, communicating test data, and passing memory test are all inherent in POST operation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. No. US 2004/0181656) as applied to claim 1 above, and further in view of Heller (Pat. No. 6,516,410).

With respect to Claim 2, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot . Stern et al. does not teach the use of CPU 64-bit MMX registers. Heller teaches the use of 64-bit MMX registers (col. 5, lines 36 & 37) during boot-up procedures. It would have been obvious, to one of ordinary skill in the art at the time of the invention, to combine the teachings of Stern et al. and Heller to speed up software performance by utilizing MMX technology to process multiple data elements in parallel.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. No. US 2004/0181656) as applied to claim 1 above, and further in view of Cox (Pat. No. 5,357,621).

With respect to Claim 3, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot . Stern et al. does not teach incrementing memory by at least one Mbyte and repeating the incrementation. Cox teaches testing of memory (col. 4, line 57) in increments of 1 megabyte blocks (col. 10, line 9) and repeating the process (col. 14, line 4). It would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teachings of Stern et

al. and Cox by choosing what is well known in the art as a reasonable increment (1 Mbyte) of memory.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. No. US 2004/0181656) and Cox (Pat. No. 5,357,621) as applied to claim 3 above, and further in view of DeRoo et al. (Pat No. 5,872,967).

With respect to Claim 4, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot. Cox teaches testing of memory (col. 4, line 57) in increments of 1 megabyte blocks (col. 10, line 9). Stern et al. and Cox do not teach a gate A20 to support the memory test. DeRoo teaches setting and resetting a gate A20 (col. 16, line 8). It would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teachings of Stern et al., Cox and DeRoo because the A20 signal allows memory above one megabyte to be accessed.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. US 2004/0181656) and Cox (Pat. No. 5,357,621), as applied to claim 3 above, and further in view of Shipman et al. (Pat. No. 5,671,413).

With respect to Claim 5, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Cox teaches testing of memory (col. 4, line 57) in increments of 1 megabyte blocks (col. 10, line 9). Stern et al. and Cox do not teach providing input/output in a protected mode. Shipman et al. teaches a method of providing basic input/output services (BIOS) in a computer by entering protected mode (fig. 9, #904) and exiting protected mode (fig.

9, #908). It would have been obvious to one of ordinary skill in the art at the time of the invention , to combine the teachings of Stern et al., Cox, and Shipman et al. such that no other processes would interfere with incrementing and testing memory.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. US 2004/0181656). as applied to claim 1 above, and further in view of Hikone et al. (Pat. No. US 6,317,853).

With respect to Claim 6, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Stern et al. does not teach use of ADD and SUB instructions and avoiding INC and DEC instructions. Hikone et al. teaches a method of generating test data (col. 1, line 11) using ADD (col. 7, line 36) and SUB (col. 7, line 38) instructions, avoiding INC and DEC instructions. It would have been obvious for one of ordinary skill in the art, at the time of the invention to combine the teachings of Stern et al. and Hikone et al. to reduce processing time through use of instructions which supports pipelining.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. US 2004/0181656) and Hikone et al. (Pat. No. US 6,317,853), as applied to claim 6 above, and further in view of Brauch et al. (U.S. Pat. No. 6,550,023).

With respect to Claim 7, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Hikone et al. teaches a method of generating test data (col. 1, line 11) using ADD (col.

7, line 36) and SUB (col. 7, line 38) instructions. Stern et al. and Hikone et al. do not teach generating test data with a boundary test routine or a stuck bit test routine. Brauch et al. teaches a method for testing memory wherein generating the test data further comprises: generating test data with a boundary test (col. 1, line 64) routine; and generating test data with a stuck bit test (col. 1, line 53) routine. It would have been obvious to one of ordinary Skill in the art at the time of the invention, to combine the teachings of Stern et al., Hikone et al., and Brauch et al. in order to conduct operational testing and to verify the integrity of the test results.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. US 2004/0181656), Hikone et al. (Pat. No. US 6,317,853), and Brauch et al. (U.S. Pat. No. 6,550,023) as applied to claim 7 above, and further in view of Vellolil et al. (Pat. Pub No. 2004/0068679).

With respect to Claim 8, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Hikone et al. teaches a method of generating test data (col. 1, line 11) using ADD (col. 7, line 36) and SUB (col. 7, line 38) instructions. Brauch et al. teaches a method for testing memory wherein generating the test data further comprises: generating test data with a boundary test (col. 1, line 64) routine; and generating test data with a stuck bit test (col. 1, line 53) routine. Stern et al., Hikone et al., and Brauch et al. do not teach executing 32-bit code. Vellolil et al. teaches a method for generating test data [0015] which comprises executing 32-bit [0005] code on the CPU. It would have been obvious

to one of ordinary skill in the art at the time of the invention, to combine the teachings of Stern et al., Hikone et al., Brauch et al., and Vellolil et al. in order to utilize data busses, registers, and address busses of the same size.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stern et al. (Pat. Pub. US 2004/0181656), as applied to claim 1 above, and further in view of Chen et al. (Pat. Pub No. 2004/0073771).

With respect to Claim 9, Stern et al. teaches a method for testing memory [0015] of an information handling system [0014] during boot or Power On Self Test (POST). Stern does not teach using the MOVNTDQ instruction to move data in 128-bit increments. Chen et al. discloses a method of testing memory wherein generating test data further comprises: using the MOVNTDQ instruction [0085] on the CPU to move test data in the memory in 128-bit [0057] increments. For the purposes of this assessment, the movq (move quad) instruction is the same as MOVNTDQ (Move Non-Temporal Double Quadword). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Stern et al. and Chen et al. to move the most data (Quadwords) with less clock cycles using 128-bit Single Instruction Multiple Data (SIMD) technology.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al. (Pat. Pub No. 2005/0081024) and further in view of Chen et al. (Pat. Pub No. 2004/0073771).

With respect to Claim 10, Khatri et al. teaches an Information Handling System comprising a CPU operable to perform instructions [0021]; random access memory to store information [0021]; firmware operable to startup CPU [0020] and instructions comprising 32-bit code [0031]; and to initiate memory test during startup [0026]. Memory test is inherently part of Power On Self Test (POST). Khatri does not teach generating test data using 128-bit SIMD registers and the Move the Non-Temporal Data Quadword (MOVNTDQ) instruction. Chen et al. teaches 128-bit SIMD [0057] registers and the move [0069] quadword [0059] instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Khatri et al. and Chen et al. to enhance performance of the information handling system by moving more data (4 32-bit words) faster (64-bits at a time vs. 32-bits).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al.(Pat. Pub No. 2005/0081024) and Chen et al. (Pat. Pub No. 2004/0073771). as applied to claim 10 above, and further in view of Chang (U.S. Pat No. 5,954,831) and Bear et al. (U.S. pat No. 6,697,978).

With respect to Claim 11, Khatri et al. teaches teaches an Information Handling System comprising a CPU operable to perform instructions [0021]; random access memory to store information [0021]; firmware operable to startup CPU [0020] and instructions comprising 32-bit code [0031]; and to initiate memory test during startup [0026]. Memory test is inherently part of Power On Self Test (POST). Chen et al. teaches 128-bit SIMD [0057] registers and the move [0069] quadword [0059]

instruction. Khatri et al. and Chen et al. do not teach performing a walking 1s and 0s routine or performing a multipattern routine. Chang teaches, under ABSTRACT, performing a walking 1s and 0s routine. Bear et al. teaches, under ABSTRACT, performing a multi-pattern routine. It would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teachings of Khatri et al., Chen et al., Chang , and Bear et al. as an efficient method for quickly and completely testing memory, function of the address decoder, and iterative changes.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al.(Pat. Pub No. 2005/0081024), Chen et al. (Pat. Pub No. 2004/0073771), Chang (U.S. Pat No. 5,954,831), and Bear et al. (U.S. pat No. 6,697,978) as applied to claim 11 above, and further in view of Korhonen (U.S. Pat. No. 7,139,954).

With respect to Claim 12, Khatri et al. teaches teaches an Information Handling System comprising a CPU [0021]; random access memory [0021]; firmware [0020] and instructions comprising 32-bit code [0031]; and to initiate memory test during startup [0026]. Chen et al. teaches 128-bit SIMD [0057] registers and the move [0069] quadword [0059] instruction. Chang teaches performing a walking 1s and 0s routine. Bear et al. teaches performing a multi-pattern routine. Khatri et al., Chen et al., Chang, and Bear et al. do not teach generating test data comprising ADD and SUB instructions and lacking INC and DEC instructions. Korhonen teaches a method for testing information handling system memory (col.1, lines 16-19) wherein instructions to generate test data comprises: using ADD and SUB instructions (col 8, lines 14-16); and

lack INC and DEC instructions. It would have been obvious to one of ordinary skill in the art ,at the time of the invention , to combine the teachings of Khatri et al., Chen et al., Chang, Bear et al., and Korhonen such that operations can be performed on source and destination operands of the same size, with only one operand in a memory location at a time, and all flags are affected.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al.(Pat. Pub No. 2005/0081024), Chen et al. (Pat. Pub No. 2004/0073771), Chang (U.S. Pat No. 5,954,831), and Bear et al. (U.S. pat No. 6,697,978) as applied to claim 11 above, and further in view of Korhonen (U.S. Pat. No. 7,139,954) as applied to claim 12 above, and further in view of Cox (Pat. No. 5,357,621).

With respect to Claim 13, Khatri et al. teaches teaches an Information Handling System comprising a CPU [0021]; random access memory [0021]; firmware [0020] and instructions comprising 32-bit code [0031]; and to initiate memory test during startup [0026]. Chen et al. teaches 128-bit SIMD [0057] registers and the move [0069] quadword [0059] instruction. Chang teaches performing a walking 1s and 0s routine. Bear et al. teaches performing a multi-pattern routine. Korhonen teaches a method for testing information handling system memory (col.1, lines 16-19) wherein instructions to generate test data comprises: using ADD and SUB instructions (col 8, lines 14-16); and lack INC and DEC instructions. Khatri et al., Chen et al., Chang, and Bear et al. and Kohonen do not teach memory testing wherein the portions are one Mbyte. Cox teaches memory testing wherein the portions are one Mbyte (col. 10, lines 5-13) in size. It would

have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachins of Khatri et al., Chen et al., Chang, and Bear et al., Kohonen and Cox to make use of what is considered, in the art, to be a reasonable portion of memory to increment.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al. (Pat. Pub No. 2005/001024) as applied to claim 10 above, and further in view of DeRoo et al. (Pat. No. 5,872,967).

With respect to Claim 14, Khatri et al. teaches an Information Handling System comprising a CPU operable to perform instructions [0021]. Khatri et al. does not teach setting, maintaining, or resetting a gate A20. DeRoo teaches an information handling system comprising instructions to: set gate A20 before generating the test data; maintain the gate A20 setting through each iterative application of the test data to the portions; and reset gate A20 upon completion of all iterative applications of the test data (col. 15, lines 21-22). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Khatri et al. and DeRoo et al. because use of an A20 gate signal provides access to memory greater than one Mbyte.

Claim15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al. (Pat. Pub No. 2005/001024) as applied to claim 10 above, and further in view of Shipman et al. (U.S. Pat No. 5,671,413).

With respect to Claim 15, Khatri et al. teaches an Information Handling System comprising a CPU operable to perform instructions [0021]. Khatri et al. des not teach entering, maintaining, and exiting a protected mode. Shipman et al. teaches an information handling system comprising instructions to: enter a protected (fig. 8, #804) mode before generating the test data; maintain the protected mode through each iterative application of the test data to the portions; and exiting the protected mode (fig. 8, #808) upon completion of all iterative applications of the test data. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Khatri et al. and Shipman et al. such that no other processes are interfering with the incrementing and testing of memory.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khatri et al. (Pat. Pub No. 2005/001024) as applied to claim 10 above, and further in view of Heller (Pat. No. 6,516,410).

With respect to Claim 16, Khatri et al. teaches an Information Handling System comprising a CPU operable to perform instructions [0021]. Khatri et al. does not teach use of CPU 64-bit MMX registers. Heller teaches an information handling system further comprising instructions to use 64-bit MMX registers of the CPU for temporary storage of test data (col. 3, lines 36-39). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Khatri et al. and Heller to utilize the enhanced performance characteristics of the MMX technology instruction parallel processing capabilities.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wynn et al. (Pub. No. US 2003/0125908) in view of Chen et al. (Pat. Pub No. 2004/0073771).

With respect to Claim 17, Wynn et al. teaches a method of testing memory at boot of an information handling system [0014] comprising initiating a memory test during POST [0042]. Initiating a memory test, generating test data, applying test data, and passing the memory test are inherent in Power On Self Tests. Wynn does not teach use of 128-bit SIMD and a MOVNDQ instruction. Chen et al. teaches a method of testing memory wherein generating test data further comprises using the movq [0085] instruction on the CPU to move test data in memory in128-bit [0057] increments. The movq (move quad) instruction is the same as MOVNTDQ (Move Non-Temporal Double Quadword). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Wynn et al. and Chen et al. to move the most data (Quadwords) with less clock cycles using Single Instruction Multiple Data (SIMD) technology.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wynn et al. (Pub. No. US 2003/0125908) and Chen et al. (Pat. Pub No. 2004/0073771) as applied to claim 17 above, and further in view of DeRoo et al. (U.S. Pat No. 5,872,967).

With respect to Claim 18, Wynn et al. teaches a method for testing memory of an information handling system [0014]. Chen et al. teaches a method of testing memory wherein generating test data further comprises using the movq [0085] instruction on the

CPU to move test data in memory in128-bit [0057] increments. Wynn et al. and Chen et al. do not teach setting, maintaining, or resetting of a gate A20. DeRoo et al. teaches a method of testing memory further comprising: setting gate A20, maintaining the gate A20 setting , and resetting gate A20 (col 16, lines 4-16). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings of Wynn et al., Chen et al., and DeRoo et al. because use of an A20 gate signal provides access to memory greater than one Mbyte.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wynn et al. (Pub. No. US 2003/0125908), Chen et al. (Pat. Pub No. 2004/0073771), and DeRoo et al. (U.S. Pat No. 5,872,967) as applied to claim 18 above, and further in view of Chang (U.S. Pat No. 5,954,831) and Bear et al. (U.S. pat No. 6,697,978).

With respect to Claim 19, Wynn et al. teaches a method for testing memory of an information handling system [0014]. Chen et al. teaches a method of testing memory wherein generating test data further comprises using the movq [0085] instruction on the CPU to move test data in memory in128-bit [0057] increments. DeRoo et al. teaches a method of testing memory further comprising: setting gate A20, maintaining the gate A20 setting , and resetting gate A20 (col 16, lines 4-16). Wynn et al., Chen et al., and DeRoo et al. do not teach performing walking 1s and 0s or performing a multi-pattern routine. Chang teaches, under ABSTRACT, performing a walking 1s and 0s routine. Bear et al. teaches, under ABSTRACT, performing a multi-pattern routine. It would have been obvious to one of ordinary skill in the art at the time of the invention, to combine

the teachings of Wynn et al., Chen et al., DeRoo et al., Chang, and Bear et al. as an efficient method for quickly and completely testing memory, function of the address decoder, and iterative changes.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wynn et al. (Pub. No. US 2003/0125908), Chen et al. (Pat. Pub No. 2004/0073771), DeRoo et al. (U.S. Pat No. 5,872,967), Chang (U.S. Pat No. 5,954,831), and Bear et al. (U.S. pat No. 6,697,978) as applied to claim 19 above, and further in view of Hikone et al. (Pat. No. US 6,317,853).

With respect to Claim 20, Wynn et al. teaches a method for testing memory of an information handling system [0014]. Chen et al. teaches a method of testing memory wherein generating test data further comprises using the movq [0085] instruction on the CPU to move test data in memory in128-bit [0057] increments. DeRoo et al. teaches a method of testing memory further comprising: setting gate A20, maintaining the gate A20 setting , and resetting gate A20 (col 16, lines 4-16). Chang teaches performing a walking 1s and 0s routine. Bear et al. teaches, under ABSTRACT, performing a multi-pattern routine. Wynn et al., Chen et al., DeRoo et al., Chang, and Bear et al. do not teach using ADD and SUB instructions.

Hikone et al. discloses a method of generating test data (col. 1, line 11) using ADD (col. 7, line 36) and SUB (col. 7, line 38) instructions. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teachings

Wynn et al., Chen et al., DeRoo et al., Chang, and Bear et al of. and Hikone et al. to eliminate idle processor time through instruction pipelining.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonard Meredith whose telephone number is 571-270-1723. The examiner can normally be reached on 7:45am - 5:15pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached on 571-272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

L.M.
LM
04/02/2007

DAVID ROBERTSON
SUPERVISORY PATENT EXAMINER